Silicon N+ P Channel Trench MOSFET

Description

HLT13NP04PF4 with dual die, P channel MOS and N channel MOS in PDFN3333-8L package, used advanced trench technology design to provide excellent $R_{DS(ON)}$ with low gate charge. It is suitable for wide variety of application.

Features

N Channel MOS:

- V_{DS} =40V, I_D =13A
- $R_{DS(ON)}$ <23mΩ @ V_{GS}=10V
- Advanced trench technology
- Low capacitance
- Low gate charge

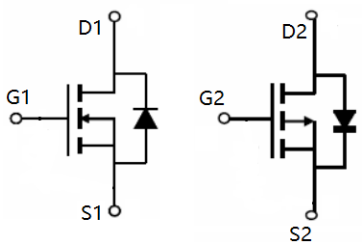
P Channel MOS:

- V_{DS}=-40V, I_D=-13A
- $R_{DS(ON)}$@V_{GS}=-10V <50mΩ
- Advanced trench technology
- Low capacitance
- Low gate charge

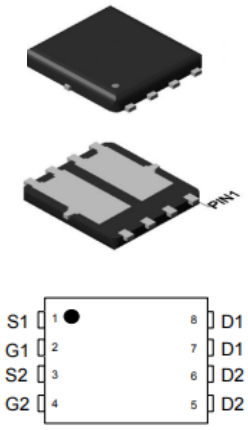
Application

- PWM application
- DC-DC converters
- Power supply
- Hard switched and high frequency circuits

Schematic diagram



Pin assignment and Top/ Bottom view



Ordering and Marking Information

Device	Package	Marking	Packing	Reel Size	Quantity
HLT13NP04PF4	PDFN3333-8L	T13NP04	Tape	13”	3K or 5K /Reel

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Max value		Unit
		N Channel	P Channel	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D	Continuous Drain Current, T_C=25℃	13	-13	A
	Continuous Drain Current, T_C=100℃	9.2	-9.2	A

I_{DM}	Pulsed Darin Current (Note1)	52	-52	A
P_D	Max Power Dissipation	15		W
T_J, T_{STG}	Operating Junction and Storage Temperature	-55~150		℃

Thermal Resistance

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note3)	8.3	℃/W

Electrical Characteristics @ T_J = 25℃ (unless otherwise specified)

Symbol	Parameter	Condition	Type	Min	Typ	Max	Unit
Static Characteristic							
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	N-Ch	40	-	-	V
		V_{GS}=0V, I_D=-250uA	P-Ch	-40	-	-	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V	N-Ch	-	-	1	uA
		V_{DS}=-40V, V_{GS}=0V	P-Ch	-	-	-1	
I_{GSSF}	Gate-Body Forward Leakage Current	V_{GS}=20V, V_{DS}=0V	N-Ch	-	-	0.1	
		V_{GS}=-20V, V_{DS}=0V	P-Ch	-	-	-0.1	
I_{GSSR}	Gate-Body Reverse Leakage Current	V_{GS}=-20V, V_{DS}=0V	N-Ch	-	-	-0.1	
		V_{GS}=20V, V_{DS}=0V	P-Ch	-	-	0.1	
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	N-Ch	1	-	2.5	V
		V_{DS}=V_{GS}, I_D=-250uA	P-Ch	-1		-2.5	
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=6.5A	N-Ch	-	17	23	mΩ
		V_{GS}=-10V, I_D=-6.5A	P-Ch	-	36	50	
		V_{GS}=4.5V, I_D=5.0A	N-Ch	-	21	30	
		V_{GS}=-4.5V, I_D=-5.0A	P-Ch	-	50	70	
gfs	Forward Transconductance	V_{DS}=5V, I_D=6.5A	N-Ch	-	10	-	S
		V_{DS}=-5V, I_D=-6.5A	P-Ch	-	11	-	
Dynamic Characteristic							
C_{iss}	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1.0MHz	N-Ch	-	960	-	pF
C_{oss}	Output Capacitance			-	85	-	
C_{rss}	Reverse Transfer Capacitance			-	68	-	

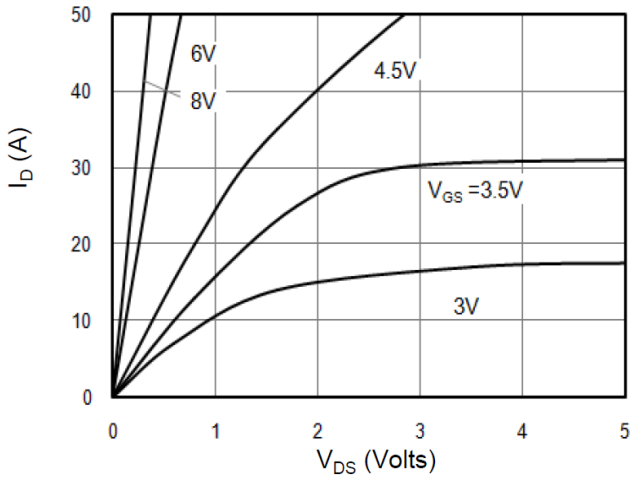
C_{iss}	Input Capacitance	V_{DS}=-20V, V_{GS}=0V, f=1.0MHz	P-Ch	-	1070	-	
C_{oss}	Output Capacitance			-	110	-	
C_{rss}	Reverse Transfer Capacitance			-	80	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=20V, V_{GS}=10V, I_D=6.5A, R_{GEN}=2.0Ω	N-Ch	-	12	-	nS
t_r	Turn-on Rise Time			-	14	-	
$t_{d(off)}$	Turn-off Delay Time			-	37	-	
t_f	Turn-off Fall Time			-	8.8	-	
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-20V, V_{GS}=-10V, I_D=-6.5A, R_{GEN}=2.5Ω	P-Ch	-	8	-	
t_r	Turn-on Rise Time			-	14	-	
$t_{d(off)}$	Turn-off Delay Time			-	23	-	
t_f	Turn-off Fall Time			-	9	-	
Q_g	Total Gate Charge	V_{DS}=20V, I_D=6.5A, V_{GS}=10V	N-Ch	-	11	-	nC
Q_{gs}	Gate-Source Charge			-	2	-	
Q_{gd}	Gate-Drain Charge			-	2.3	-	
Q_g	Total Gate Charge	V_{DS}=-20V, I_D=-6.5A, V_{GS}=-10V	P-Ch	-	20	-	
Q_{gs}	Gate-Source Charge			-	3.7	-	
Q_{gd}	Gate-Drain Charge			-	4.6	-	
Drain-Source Diode Characteristics							
V_{SD}	Diode Forward Voltage (Note3)	V_{GS}=0V, I_S=6.5A	N-Ch	-	-	1.2	V
		V_{GS}=0V, I_S=-6.5A	P-Ch	-	-	-1.2	
trr	Reverse Recovery Time	I_F=6.5A, di/dt=100A/us	N-Ch	-	20	-	nS
		I_F=-6.5A, di/dt=100A/us	P-Ch	-	30	-	
Qrr	Reverse Recovery Charge	I_F=6.5A, di/dt=100A/us	N-Ch	-	12	-	nC
		I_F=-6.5A, di/dt=100A/us	P-Ch	-	20	-	

Noted:

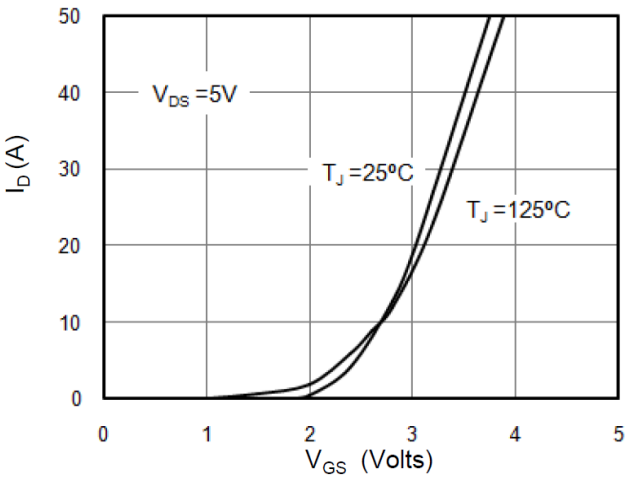
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

Electrical Characteristics Diagrams

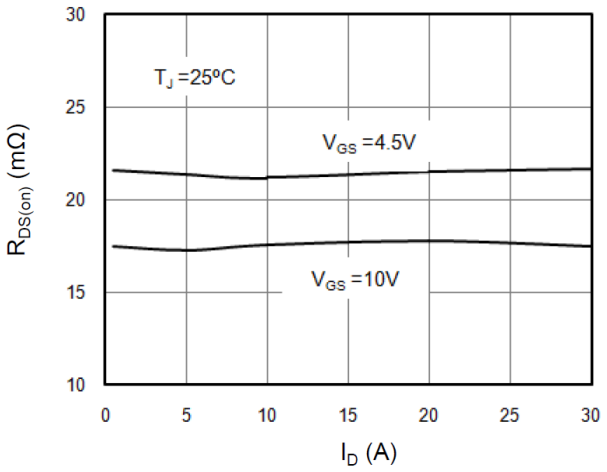
N Channel MOS:



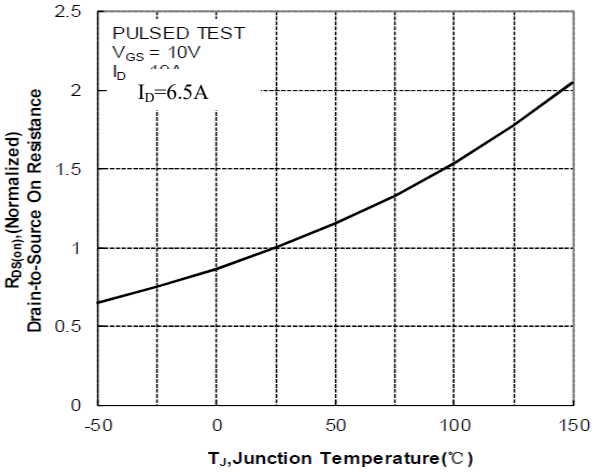
Typical Output Characteristics



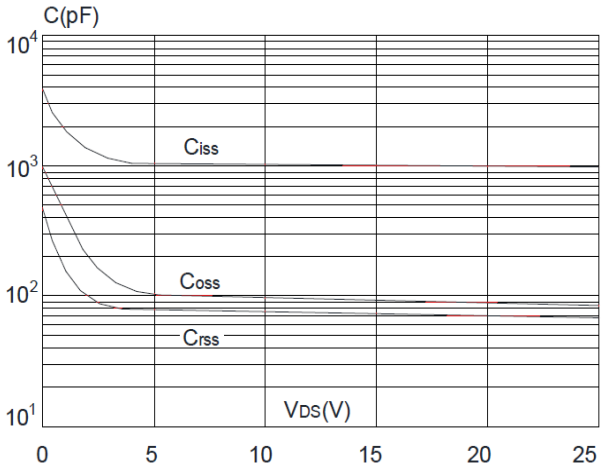
Typical Transfer Characteristics



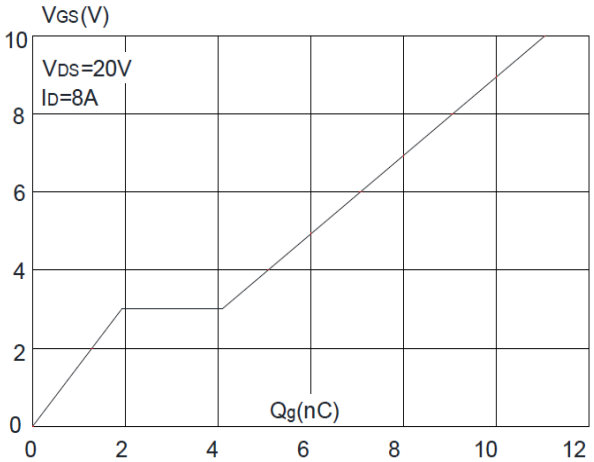
Drain-to-Source On Resistance vs Drain Current



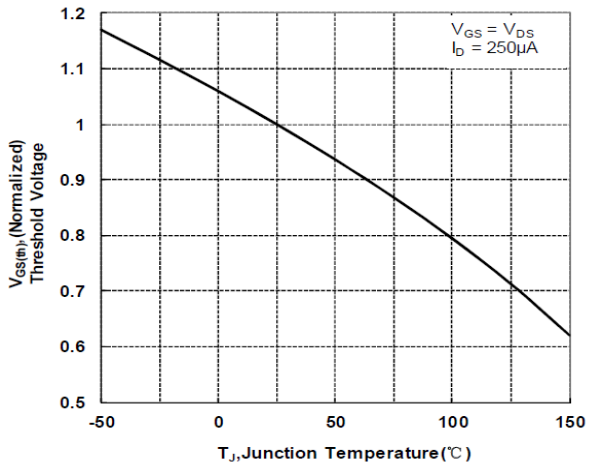
Normalized On Resistance vs T_J



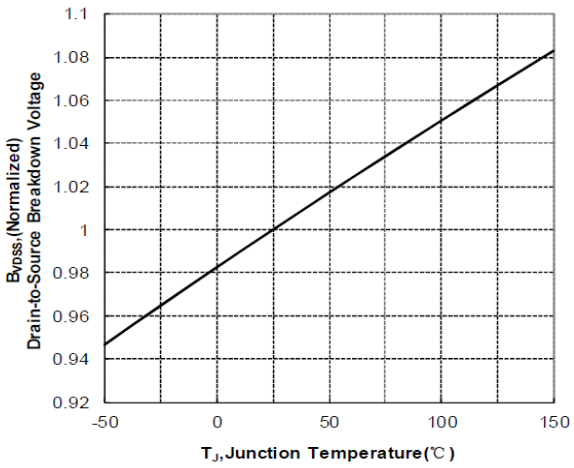
Capacitance Characteristics



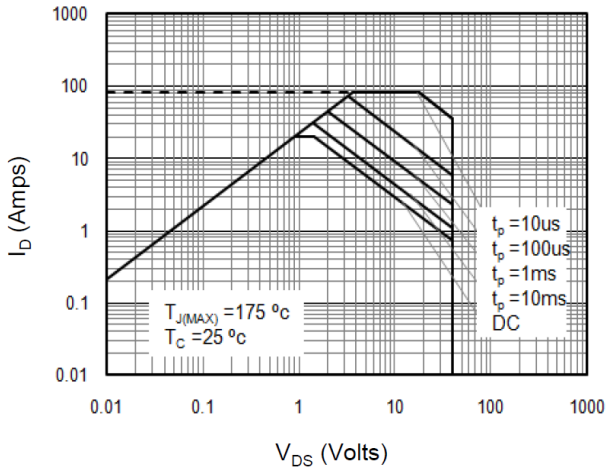
Gate Charge



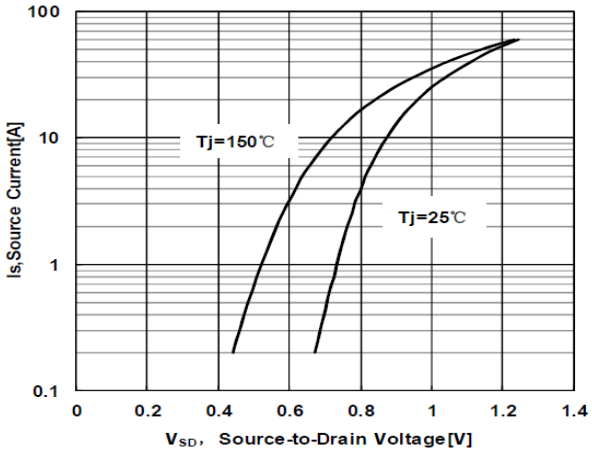
Normalized Threshold Voltage vs T_J



Normalized Breakdown Voltage vs T_J

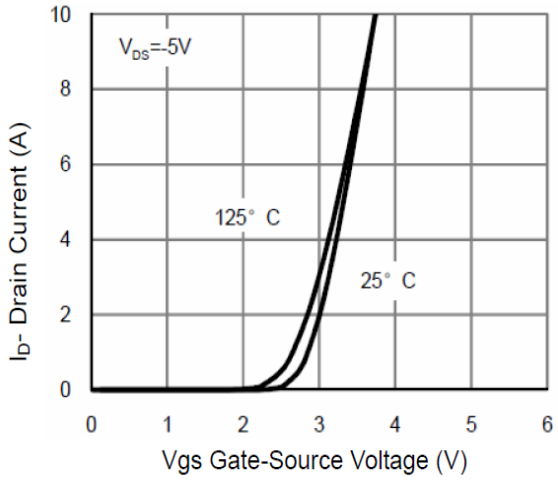


Safe Operation Area

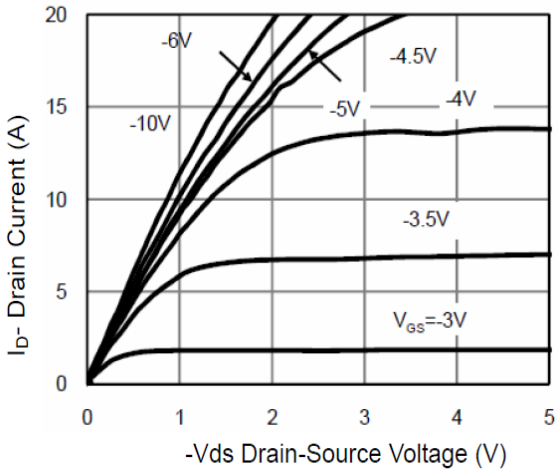


Source- Drain Diode Forward

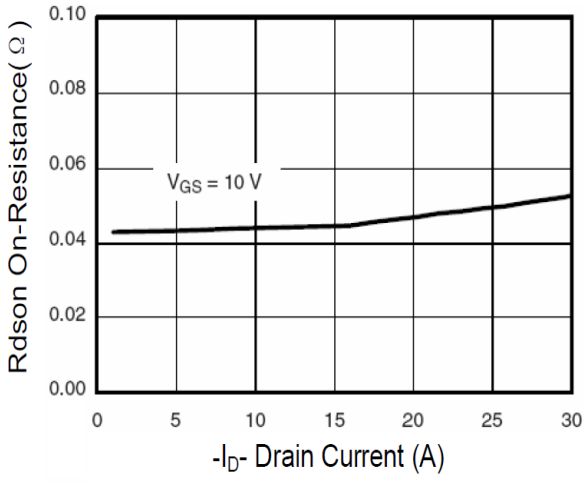
P Channel MOS:



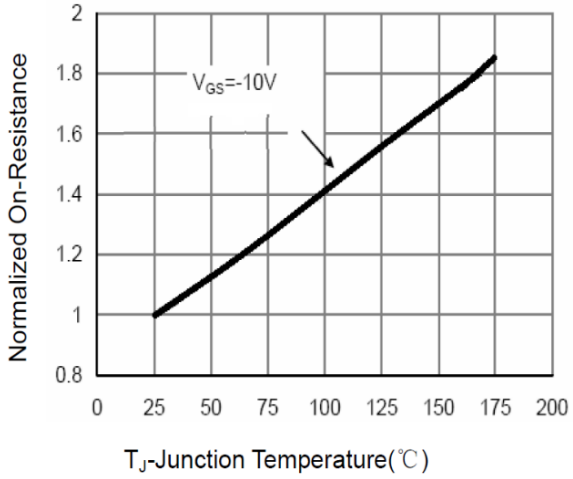
Transfer Characteristics



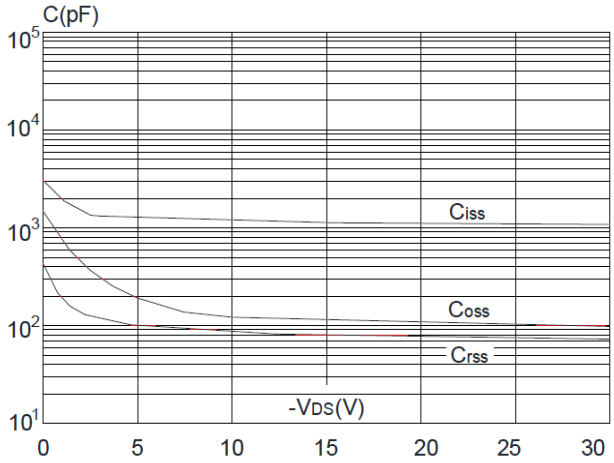
Output Characteristics



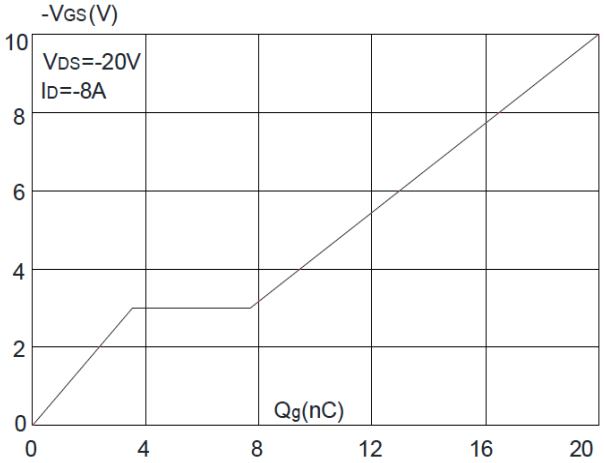
Rdson vs Drain Current



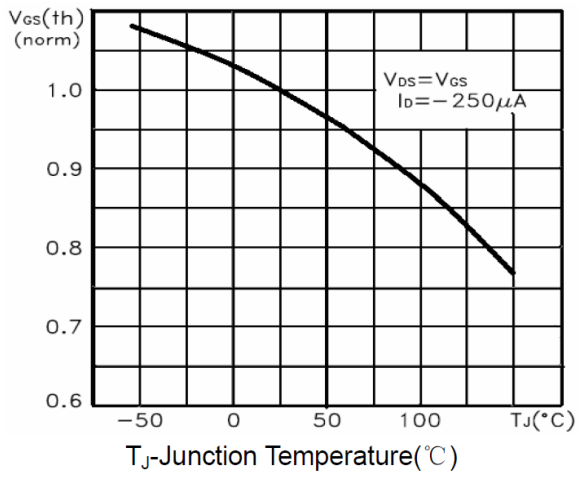
Rdson vs Temperature



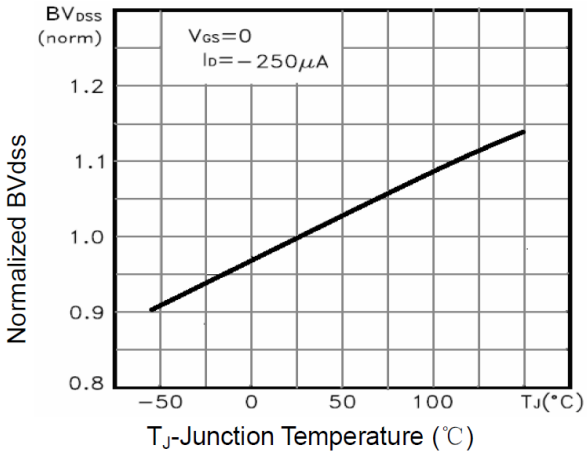
Capacitance vs Vds



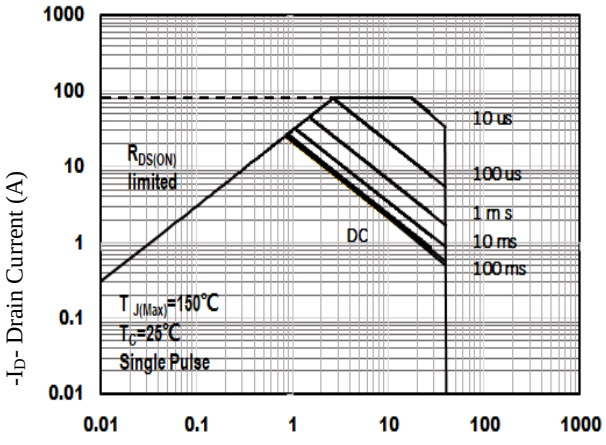
Gate Charge



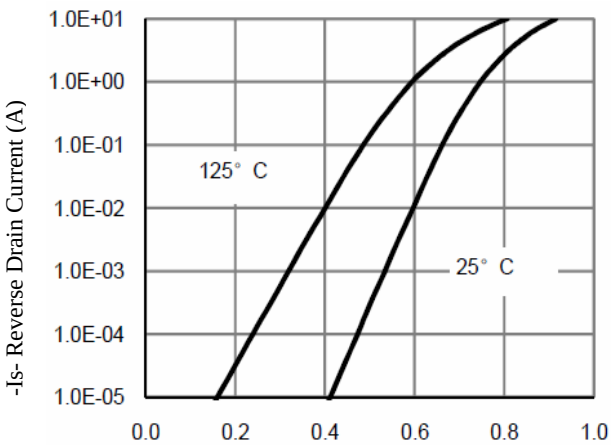
Normalized Threshold Voltage vs T_J



Normalized Breakdown Voltage vs T_J

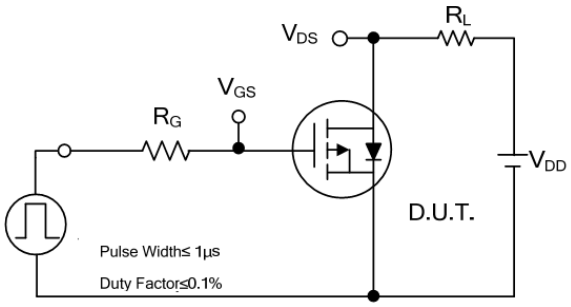


Safe Operation Area

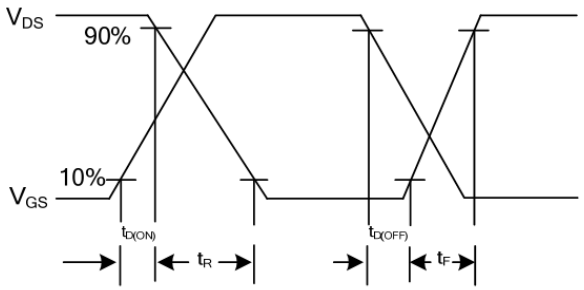


Source- Drain Diode Forward

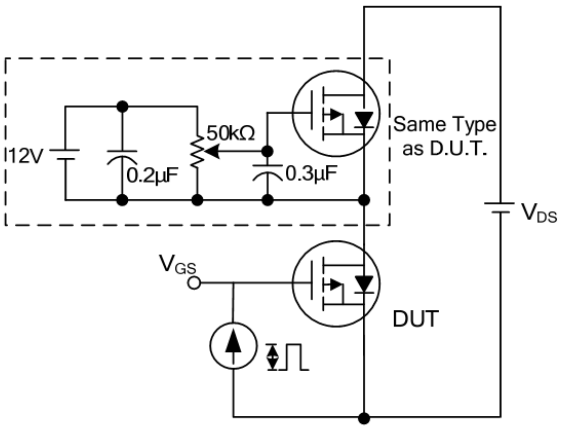
Test Circuit and Waveform



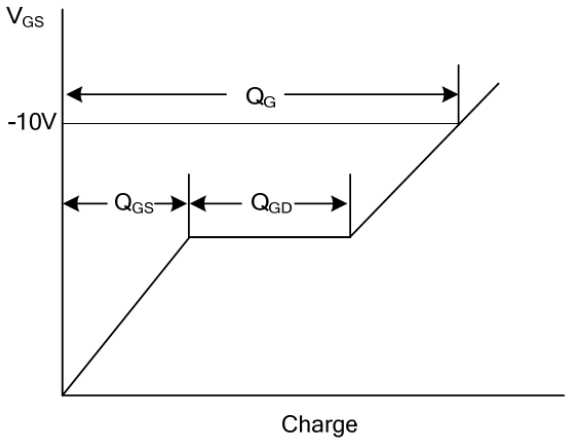
Switching Test Circuit



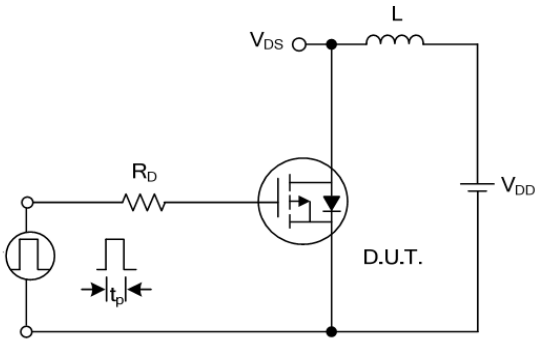
Switching Waveforms



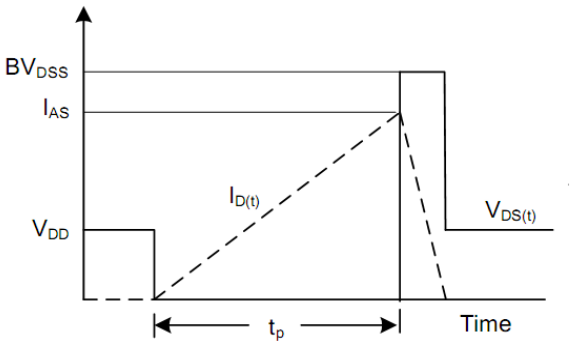
Gate Charge Test Circuit



Gate Charge Waveform



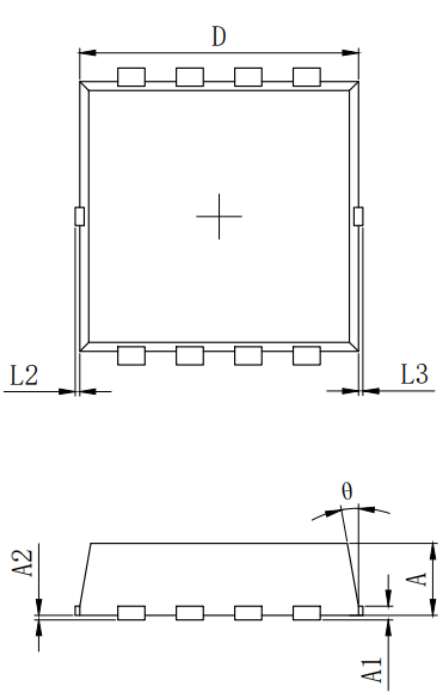
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Package Information

PDFN3333-8L Package



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.700	0.800	0.900
A1	0.152 REF.		
A2	0~0.05		
D	3.000	3.100	3.200
D1	0.935	1.035	1.135
D2	0.280	0.380	0.480
E	2.900	3.000	3.100
E1	3.150	3.300	3.450
E2	1.535	1.735	1.935
b	0.200	0.300	0.400
e	0.550	0.650	0.750
L	0.300	0.400	0.500
L1	0.180	0.330	0.480
L2	0~0.100		
L3	0~0.100		
H	0.315	0.415	0.515
θ	8°	10°	12°